CLAIMS

1. A method of distinguishing a dummy feature from a main feature, the method comprising:

selecting a mask layer;

providing a technique to identify the dummy feature on the mask layer; and

applying the technique to the selected mask layer.

2. The method of Claim 1, wherein the technique includes determining at least one of a size of a feature, a shape of a feature, a pattern from multiple features, and a proximity of a feature to another feature.

3. The method of Claim 1, further including using information from at least one other mask layer to use in the technique.

4. The method of Claim 3, wherein the information includes at least one of connectivity between the selected mask layer and the at least one other mask layer, and a functional association between the selected mask layer and the at least one other mask layer.

5. The method of Claim 1, wherein the method is performed during at least one of optical proximity correction, placement of phase-shifting structures, mask fabrication, mask inspection, and mask repair.

6. An automated method of processing a mask layer for manufacturing an integrated circuit, the method comprising:

identifying a plurality of main features and at least one dummy feature in the mask layer; and

providing the processing only to the plurality of main features.

7. The method of Claim 6, wherein processing includes at least one of correcting for optical proximity, providing phase-shifting structures, and using a user input regarding at least one of a main feature and a dummy feature.

8. The method of Claim 6, wherein processing is performed during at least one of fabrication of a mask, inspection of a mask, and repair of a mask.

9. The method of Claim 6, wherein identifying includes applying at least one of a multiple layer technique and a geometry technique.

10. The method of Claim 6, wherein identifying includes determining a size of a feature on the mask layer, a shape of a feature on the mask layer, a pattern from multiple features on the mask layer, and a proximity of a feature to another feature on the mask layer.

11. The method of Claim 6, wherein identifying includes using information from at least one other mask layer for the integrated circuit.

12. The method of Claim 11, wherein the information includes at least one of connectivity between the mask layer and the at least one other mask layer, and a functional association between the mask layer and the at least one other mask layer.

13. A mask for transferring a pattern to an integrated circuit layer, the mask comprising:

a plurality of main features; and

at least one dummy feature, wherein only the main features reflect post-layout processing.

14. The mask of Claim 13, wherein the post-layout processing includes at least one of optical proximity correction, placement of phase-shifting structures, and defect correction.

15. The mask of Claim 13, wherein at least one of the plurality of main features includes an assist bar.

16. The mask of Claim 13, wherein the at least one dummy feature provides at least one of mechanical support for the integrated circuit layer, resolution improvement of a main feature for the integrated circuit layer, a test structure for the integrated circuit layer, and a marking for the integrated circuit layer.

17. The mask of Claim 13, wherein a main feature is distinguished from a dummy feature by combining information from at least two mask layers.

18. The mask of Claim 17, wherein the information includes at least one of connectivity information and functional association information.

19. The mask of Claim 13, wherein a main feature is distinguished from a dummy feature by information on the mask layer.

20. The mask of Claim 19, wherein the information includes at least one of a size of a feature, a shape of a feature, a pattern of multiple features, and a proximity of one feature to another feature.

21. The mask of Claim 13, wherein a main feature is distinguished from a dummy feature by information on the mask layer and on at least one other mask layer.

22. The mask of Claim 21, wherein the information includes at least two of feature connectivity, feature association, feature size, feature shape, feature pattern, and feature proximity.

23. A system for processing a mask layer for an integrated circuit, the system comprising:

means for receiving information regarding a feature on the mask layer;

means for determining the feature is one of a main feature and a dummy feature based on the information; and

means for identifying the feature as appropriate for further processing if the feature is a main feature and as inappropriate for further processing if the feature is a dummy feature.

24. The system of Claim 23, wherein the means for determining includes at least one of means for receiving user input regarding the technique, means for determining a feature size, means for determining a feature shape, means for determining a pattern from multiple features, and means for determining a proximity of the feature to another feature.

25. The system of Claim 23, wherein the means for determining includes means for using information from at least one other mask layer for the integrated circuit.

26. The system of Claim 25, wherein the means for determining includes at least one of means for using connectivity information between the mask layer and the at least one other mask layer, and means for using an association between the mask layer and the at least one other mask layer.

27. The system of Claim 23, further including means for processing the mask layer.

28. The system of Claim 27, wherein the processing includes at least one of optical proximity correction, placement of phase-shifting structures, raster scanning, vector scanning, feature inspection, and feature repair.

29. An integrated circuit comprising:

a plurality of layers, wherein at least one layer includes:

a plurality of main features; and

at least one dummy feature, wherein only the main features reflect post-fabrication processing.

30. The integrated circuit of Claim 29, wherein the post-fabrication processing includes defect correction.

31. The integrated circuit of Claim 29, wherein the at least one dummy feature includes at least one of a mechanical support for the layer, a test structure for the layer, and a marking for the layer.

32. The integrated circuit of Claim 29, wherein a main feature is distinguished from a dummy feature by combining information from at least two mask layers.

33. The integrated circuit of Claim 32, wherein the information includes at least one of connectivity information and functional association information.

34. The integrated circuit of Claim 29, wherein a main feature is distinguished from a dummy feature by information on a mask layer.

35. The integrated circuit of Claim 34, wherein the information includes at least one of a size of a feature, a shape of a feature, a pattern of multiple features, and a proximity of one feature to another feature.

36. The integrated circuit of Claim 29, wherein a main feature is distinguished from a dummy feature by information on a mask layer and on at least one other mask layer.

37. The integrated circuit of Claim 36, wherein the information includes at least two of feature connectivity, feature functionality, feature size, feature shape, feature pattern, and feature proximity.

38. A program storage device readable by a machine, tangibly embodying a program of instructions executable by said machine to perform method steps to analyze a mask layer for an integrated circuit, the method comprising:

providing a technique to distinguish a main feature from a dummy feature in the mask layer; and

applying the technique to the mask layer.

39. The program storage device of Claim 38, further including means for receiving user input regarding the technique.

40. The program storage device of Claim 38, wherein the technique includes at least one of determining a feature size, a feature shape, a pattern from multiple features, and a proximity of a feature to another feature.

41. The program storage device of Claim 38, wherein the technique further includes using information from at least one other mask layer for the integrated circuit.

42. The program storage device of Claim 41, wherein the information includes at least one of connectivity between the mask layer and the at least one other mask layer, and a functional association between the mask layer and the at least one other mask layer.

43. A computer program product comprising:

a computer usable medium having a computer readable program code embodied therein for causing a computer to analyze a mask layer for an integrated circuit, the computer readable program code comprising:

computer readable program code that receives information regarding a feature on the mask layer;

computer readable program code that determines the feature is one of a main feature and a dummy feature based on the information; and

computer readable program code that identifies the feature as appropriate for further processing if the feature is a main

feature and as inappropriate for further processing if the feature is a dummy feature.

44. The computer program product of Claim 43, further including computer readable program code that receives user input regarding the technique.

45. The computer program product of Claim 43, further including computer readable program code that determines at least one of a feature size, a feature shape, a pattern from multiple features, and a proximity of the feature to another feature.

46. The computer program product of Claim 43, further including computer readable program code that uses information from at least one other mask layer for the integrated circuit.

47. The computer program product of Claim 46, further including computer readable program code that uses at least one of connectivity information between the mask layer and the at least one other mask layer, and a functional association between the mask layer and the at least one other mask layer.

48. A method of inspecting a mask for defects, the mask including a plurality of features, the method comprising:

reading a mask data preparation format file;

identifying dummy versus non-dummy features using the mask data preparation format file; and

inspecting only non-dummy features.

49. The method of Claim 48, wherein identifying includes determining at least one of a size of a feature, a shape of a

feature, a pattern from multiple features, and a proximity of a feature to another feature.

50. The method of Claim 48, wherein identifying includes using information from at least one other mask.

51. The method of Claim 50, wherein the information includes at least one of connectivity and a functional association between mask layers.

52. The method of Claim 48, further including marking only the non-dummy features for repair.

53. A mask used in a lithographic process, the mask comprising:

a plurality of dummy features having uncorrected defects.

54. The mask of Claim 53, wherein the plurality of dummy features provide at least one of mechanical support, resolution improvement, a test structure, and a marking.

55. A method of conserving resources in a computer system during optical proximity correction (OPC) of a layout of an integrated circuit (IC), the method comprising:

identifying dummy versus non-dummy features from the layout; and

expending resources for OPC only on non-dummy features.

56. The method of Claim 55, wherein identifying includes determining at least one of a connectivity of features, a functional association of features, and a geometrical description of features.

57. A method of preparing an integrated circuit (IC) for fabrication, the method comprising:

separating a layout of the IC into a plurality of dummy features and a plurality of main features;

processing a subset of the plurality of main features, excluding the dummy features, for definition with optical proximity correction (OPC);

processing a subset of the plurality of main features, excluding the dummy features, to provide OPC; and

generating a data file including OPC information for use in manufacturing a mask for at least one layer of material defined by the layout.

58. The method of Claim 57, wherein the data file includes a first set of instructions for transferring the dummy features to the mask using a first accuracy and a second set of instruction for transferring the main features to the mask using a second accuracy.

59. The method of Claim 58, wherein the first accuracy includes a first beam size and the second accuracy includes a second beam size, and wherein the first beam size is greater than the second beam size.

60. The method of Claim 57, further comprising:

processing a subset of the plurality of main features, excluding the dummy features, for defining phase shifting regions;

processing a subset of the plurality of main features, excluding the dummy features, to provide phase shifting regions, wherein the data file includes phase shifting region information.

61. The method of Claim 60, further comprising:

using the mask to fabricate the IC;

identifying dummy versus main features on the mask from the data file;

inspecting locations on the mask corresponding to locations with main features, excluding the dummy features; and

correcting defects at locations on the mask corresponding to locations with main features, excluding the dummy features.

62. A computer program product including a computer usable medium having a computer readable program code embodied therein for causing a computer to generate a simulated stepper image, the computer readable program code comprising:

computer readable program code that detects dummy features from an input data file; and

computer readable program code that marks the dummy features.

63. The computer program product of Claim 62, wherein the computer readable program code that marks the dummy features provides at least one of a predetermined color and a predetermined shading of the dummy features on the simulated stepper image.

64. The computer program product of Claim 62, wherein the computer readable program code that marks the dummy features omits the dummy features on the simulated stepper image.

65. The computer program product of Claim 62, wherein the computer readable program code that marks the dummy features

expends less processing resources on simulating the dummy features than on non-dummy features.